SERIAL COMMUNICATION PROTOCOL IMPROVES DATA ACQUISITION AND CONTROL SYSTEM COST AND PERFORMANCE

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CONVENTIONAL ANALOG DATA ACQUISITION SYSTEM

Process Control, Environmental Energy Management and the host of many other digitally controlled data acquisition systems currently bring analog data from multiple remote sensor locations to a centrally located host computer via dedicated lines per sensor, there to be converted from analog to digital. (Figure 1). This point-to-point wiring of many analog signals in many ways resembles that of the conventional all-analog system it replaced. In most cases when the analog signal from a transducer was some distance away, the signal was conditioned with an analog 4 to 20 mA current loop format in an attempt to reduce the effects of cable resistance and noise pick up. Even with expensive coaxial cable, only partial relief from industrial EMI noise problems were realized. Also, when analyzing the cost of a large, multiple point system where dedicated wires per sensor is required, it is commonly found that the installation cost of cable alone can frequently exceed half of the total system cost. Therefore, any improvement over the single dedicated cable per signal could have a significant impact on cost.

Another often overlooked consideration is the inability of the conventional system to be easily expanded or relocated at some unspecified future time. Although this can be partically accommodated by laying a number of extra unused cables, most modifications usually require routing of cables to new locations and possibly new conduit. This can be particularly costly and difficult when modifying a plant which must remain in operation during the installation or system update.

UTILIZING A SERIAL DIGITAL PARTY LINE ARCHITECTURE

Present availability of low cost A/D converters, such as the Intersil ICL7109 CMOS 12 bit A/D converter, enables reconsideration of traditional system architecture. The new configuration would locate the A/D converter as close as possible to the transducer, thus greatly enhancing the performance while reducing the noise pick-up on long analog lines. While each A/D converter's output could be transmitted by individual parallel cables to be digitally multiplexed at the central location, a lower cost approach suggests a more efficient structure.

By converting each A/D's output immediately along with any digital I/O for monitoring or control to a serial digital format and placing the data on a common serial BUS, the over-all cost of system wiring is dramatically reduced (Table 1). In addition, the system could be easily expanded or reconfigured with minimum impact of the already installed wiring.

This system architecture offers a decided improvement in both accuracy and cost of installation (Table II). What is required to successfully implement this architecture is an efficient method of supervising the transmission of data on the serial BUS.

SERIAL PROTOCOL

A key element of the serial data transmission concept is the choice of protocol. The protocol chosen must provide for the following items:

Transmit or Receive Indicator
Remote's Address
Command Word
Data Word
Error Detection
Sychronization

Several serial data link protocols have been in common use: These include Bisync, SDLC, HDLC and Packed ASCII. The first three of these have been developed primarily to service high data rates between two fixed stations. Through use of Cyclic Redundancy checking (C.R.C.), the error rates of these first three protocols can be made quite low. Since our system, however, will be transmitting many short messages to and from the various remote locations, it is important that the ratio of message overhead bits to data bits be optimized. Table III compares the major characteristics of these protocols with packed ASCII. Packed ASCII has the advantage of being readily transmitted by existing hardware such as standard UARTS; but the format is still low on efficiency and less effective on error checking. It can be seen in Table III that each of the protocols shown requires a large amount of overhead to transmit 16 bits of data, which is a typical data size in most process control, environmental engergy management or general purpose data monitoring and control systems.

Ideally, all tasks related to the data

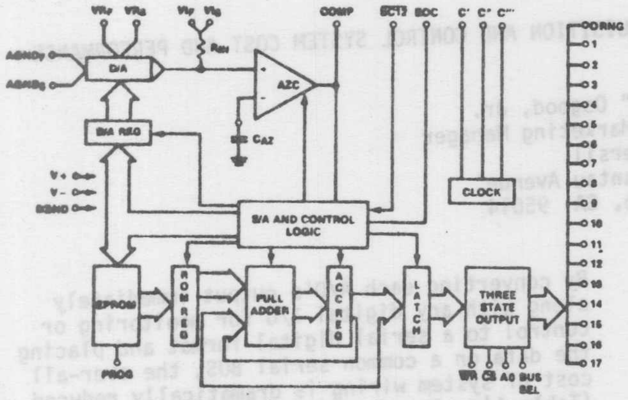


Fig. 23 Block diagram of the A/D chip.

At the $(n)^{th}$ step of the conversion, two trial bits are switched in together, -the $(n)^{th}$ and the $(n+4)^{th}$. If the comparator decides to "kkep", then the $(n)^{th}$ bit stays and the $(N+4)^{th}$ bit is removed. If the decision is "drop" then both bits are removed. An erroneous decision to "keep" is corrected by the removal of the $(n+4)^{th}$ bit which is about 8% of the pair value. On the other hand a comparator error to "drop"- the $(n)^{th}$ bit is corrected later since the succeeding bits in a 1.85 radix D/A add up to about 118% of the $(n)^{th}$ bit. With this algorithm the comparator input needs to settle to only about 3 time-constants compared to more than 12 time-constants normally required for 14-bit accuracy, (see Fig. 24).

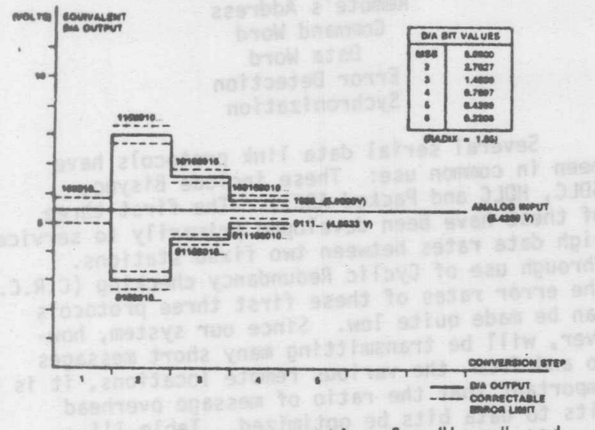


Fig. 24 Error correction for "keep" and "drop" errors.

A comparator decision to "keep" causes the corresponding bit value to be accessed from the EPROM and added into the accumulator register, while a "drop" decision leaves the accumulator contents unchanged. At the end of the conversion the accumulator contains the sum of the values of the bits that were "kept", which represents the input voltage. 17-bits of internal resolution are needed to compensate for accumulated errors that can result from the successive additions of the bit values. The result is rounded-off to 14-bits at the end of the conversion.

The chip contains all necessary logic for direct interface to most popular microprocessers, their derivatives and DMA controllers. Since these parts are also programmed after packaging, calibration is unaffected by assembly or burn-in drifts. The redundancy prevents occurance of missing codes and results in significant yield improvement to higher accuracies. This new technique makes use of the advantages of the CMOS technology, providing higher resolution through digital output correction and higher conversion speeds through error-correction, redundancy and special comparator circuit techniques.

I think it should be obvious that these are just the beginnings of an invasion of analog and conversion circuits by digital techniques. Combinations such as A/D with switching, computing and storage elements on a single die, open a fasinating vista of possibilities for the furture. The low power dissipation and high performance capabilites of CMOS technology, together with its versatility, ensure that it will play a major role in such developments.

transfer on the serial BUS should be supervised by the system architecture, thus releaving the host computer from this task. This has the further important benefit of eliminating the software required to supervise the serial BUS, being done in firmware by the BUS interface circuit. All the host computer need do is request data from a particular data point by issuing a remote station address and control word command. Additionally, the remote station could provide digital I/O for control purposes.

A PRACTICAL REMOTE DATA ACQUISITION AND CONTROL SYSTEM

A system employing the above serial data principles has been developed and is currently manufactured and marketed by Intersil, Inc. under the trade name REMDACS. The task of formulating the command data from the host computer and supervision of the remote stations has been accomplished by firmware placed into the ROM of an 8048 type 8 bit microcomputer located at each remote station and host computer Receiver/Transmitter.

Figure 3 shows the structure of the REMDACS dual message format-a 24 bits message for a moderate data integrity high speed and a 44 bit message for highest data integrity but lower speed. These words contain a high ratio of data bits to overhead with error checking methods sufficient for the word length. These message formats can be configured as address and control commands (transmit) or as the data (response) from a remote station. Note that the first bit after the start bit indicates whether the message format will be 24 or 44 bits, therefore both word lengths can be used on the same serial BUS. The next bit indicates whether the word is a command from the Receiver/ Transmitter or a response from a remote, thereby allowing the unaddressed remotes to return to standby. The next 16 (or 32 for the 44 bit message) bits can be used for addressing and control for a command from the Receiver/ Transmitter, or as the data field in a remote station response word. As it can be seen, the ratio or data to overhead is superior to any of the protocols shown in Table III.

Figures 4, 5 and 6 show the structure of the analog remote 24 bit messages. The bits marked with a "T" are added and removed by the firmware on the Receiver/Transmitter and are totally transparent to the host computer. The host computer transfers only a 16 bit control word to the Receiver/Transmitter. The Receiver/ Transmitter card has a general purpose parallel port to interface to the host computer data BUS and is capable of outputting both 24 and 44 bit messages, thus one Receiver/Transmitter card can supervise up to 256 24 bit remotes and up to 256 44 bit remotes (not presently available) similtaneously on the same twisted pair. Remotes can be miles from the host computer (Receiver/ Transmitter). Distance limitations are regulated by the drive current of the Opto isolated receiver at each remote and the resistance of the twisted pair. Communication rates are from 150 baud to 4800 baud allowing 95 station acquisitions per second at the maximum rate. This is more than adequate for most real-time process systems. An RS232C interface card is available to connect to virtually any computer. Dedicated Receiver/Transmitter cards are also available for both STD BUS and Multibus, others are planned for the near future.

The 24 bit control word (Figure 4) contains 8 bits of remote station address, 4 bits of control information and 4 bits of digital I/O which can be used for example, to address a multiplexer.

Figure 5 shows the 24 bit analog remote station response message format which contains a 12 bit data field for the A/D converter plus 4 bits of channel address. An additional feature is indicated by Figure 6: This is a remote status message intended to facilitate system diagnostics, enabling system trouble shooting under software control. This is an extremely powerful advantage in maintaining a system spread out over a large geographic area. Figures 7, 8 and 9 show the structure of the digital remote 24 bit message.

INTERSIL REMDACS REMOTES

Three types of analog sensing remote cards have been developed; one contains a 16 channel low level multiplexer (2 X 1H6108) and all signal conditioning for interfacing to conventional 4 to 20 mA analog transmitters. The second card has been optimized for energy management applications and contains the 16 channel multiplexer and all signal conditioning for utilizing the AD590 two wire current loop silicon temperature sensor. The third card is intended for general low level analog signal acquisition and contains a 16 channel low leakage multiplexer that can be configured as either 16 single-ended inputs or 8 differential inputs plus on-board pre-amplifier(s) for scaling the input range from 10mV full scale and up. The 12 bit accurate CMOS A/D converter (ICL7109) provides high common mode and normal mode rejection, very high input impeadance, making external signal conditioning unnecessary for most applications.

For digital sense inputs or control signal outputs, a digital remote station has been developed. It employs a carefully-conceived combination of general-purpose master digital remote station complemented by three types of peripheral cards. The master digital remote handles all communication with the Receiver/ Transmitter while the peripheral cards serve specific monitoring and control functions.

Available are 16 digital inputs, 16 digital outputs (CMOS and Darlington-Pairs) and 4 additional points which can serve as either input or output. Like the analog cards, the general-purpose digital I/O card has complete message formatting, error-checking and isolated Receiver/Driver circuits for communicating with the Receiver/Transmitter. All remotes operate from either 24V AC or 8 to 20V DC.

DIGITAL PERIPHERALS

Several peripheral cards have been developed to support the master general-purpose digital I/O remote station with more to be available soon. The present cards are 8 channel electro-mechanical relays and 8 channel solid-state relays with LED status indication; 4 channel electro-mechanical and solid-state relays with switch over-ride, switch position read-back and LED status, plus an 8 channel active logic input card for AC/DC voltage detection from 5V to 230V RMS. A universal breadboard card is also available.

EASY INSTALLATION

Each REMDACS II remote card is compatible with the REMDACS II mother board termination system. The mother boards are divided into two basic modular interconnect systems: Analog and Digital. The analog mother board is available in one through four slots, and the digital mother board is available in two through five slots. Both analog and digital mother boards are compatible allowing easy mix and match expansion to the 256 remote stations per twisted pair (per Receiver/Transmitter). Edge connectors and card guides are provided for seating the cards and 3-terminal Weidmuller Barrier connectors are provided for direct and easy interface with external signals. For interface between cards, ribbon connectors are available. Electrical and mechanical connectors are also provided to allow interconnects between multiple analog and digital mother boards. All connectors are UL and CSA approved.

SUMMARY AND CONCLUSION

The low parts count and use of inexpensive industrial grade components allows a low manufacturing cost. This, combined with the savings in installation of cable make the REMDACS system a very attractive alternative to the conventional one-cable per analog sensor data acquisition system. In addition, the REMDACS analog remote accuracy of 0.02% is roughly an order of magnitude better than most conventional systems which are many times more costly. Plus the fact that communicating serially through a single twisted pair of wires has been shown to improve data integrity and generally reduces installation costs. An additional benefit is the ease in which the serial data may be transmitted via phone, microwave, and fiber optics.

The party-line system architecture of REMDACS allows the wiring path to be arbitrary, further minimizing total cable length and permitting additional remote stations to be added at any time and at any place on the twisted pair. It is anticipated that the superior performance of REMDACS and the strong economic advantages of this type of system structure will cause rapid adoption of the serial remote data acquisition and control concept for many industrial distributed applications.

TABLE I

CABLE COST COMPARISON EXAMPLE

Assume 16 data points located on 100' radius circle.
Center of circle located 1000' from computer.

A. Conventional point-to-point system--
16 cables X approximately 1000' ft. runs =
16,000 cable ft. at $5/ft. = $80,000.

B. Serial data system--16 X 100' + 1,000' =
2,600 cable ft. at $5/ft. = $13,000.

Net Savings-- $67,000.

Note: Cost of cable per foot varies widely with type of cable, installation codes and practices; however this example is typical of many process systems.

TABLE II

ADVANTAGES OF REMOTE SERIAL DATA ACQUISITION AND CONTROL SYSTEM

Improved system accuracy-- no signal degradation
Reduced total conduit length-- minimizes installation cost
Single twisted pair cable-- replaces multiple cables/coax
Easily expanded-- add stations at any time
Easily isolated-- interfaces to fiber optics or opto-isolators, radio link
Installs using existing wiring-- use an existing twisted pair
Allows two-way communication-- acquisition and control on same cable

TABLE III

COMPARISON OF FOUR SERIAL DATA LINK PROTOCOLS[1]

	BISYNC	SDLC	HDLC	PACKED ASCII
Full Duplex	No	Yes	Yes	Yes
Half Duplex	Yes	Yes	Yes	Yes
Asynchronous	No	No	No	Yes
Error Detection	VRC,CRC-16	CRC-CCITT	CRC-CCITT	Parity
Min Message Length in Bits for 8 bit address, 8 bit control, 16 bit data	12X8	8X8	8X8	4X11
Hardware Requirements	Complex	Complex	Complex	Simple

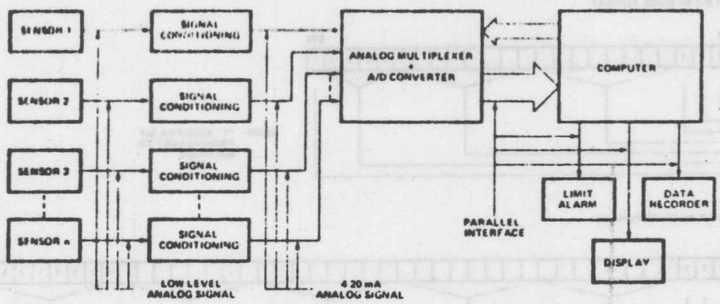


Figure 1. CONVENTIONAL DATA ACQUISITION SYSTEM.
One cable pair is used per analog channel.

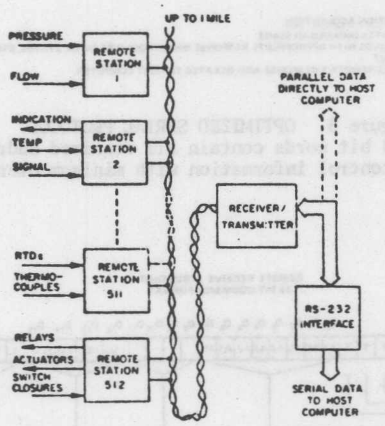
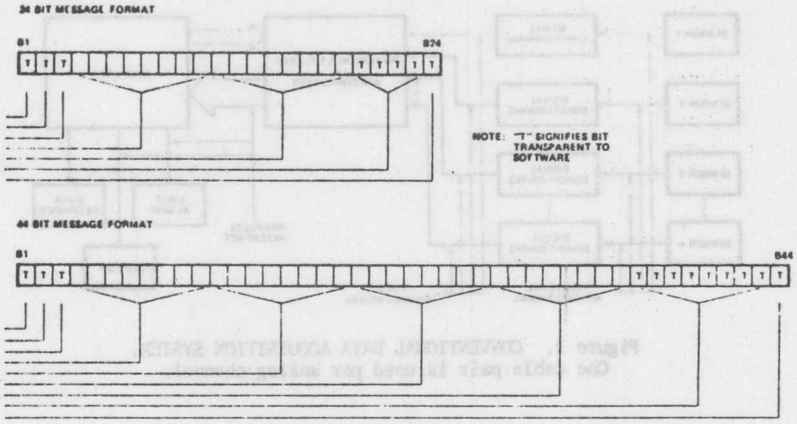


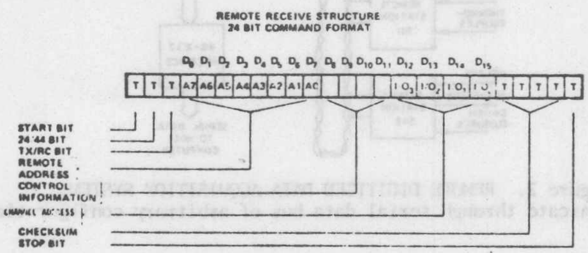
Figure 2. REMOTE DIGITIZED DATA ACQUISITION SYSTEM.
ADCs communicate through serial data bus of arbitrary configuration.



NORMAL SEQUENCE FOR REMOTE STATION ACQUISITION

1 RECEIVER-TRANSMITTER TRANSMITS COMMAND MESSAGE.
2 REMOTE STATION SELECTED RESPONDS WITH APPROPRIATE RESPONSE WHICH COULD BE DATA, STATUS, ETC. BEFORE RECEIVER-TRANSMITTER TIMES OUT
3 RECEIVER-TRANSMITTER RECEIVES REMOTE'S RESPONSE AND RELATES TO HOST COMPUTER.

Figure 3. OPTIMIZED SERIAL PROTOCOL.
24 and 44 bit words contain all required address, data and control information with minimum overhead.



ADDRESS

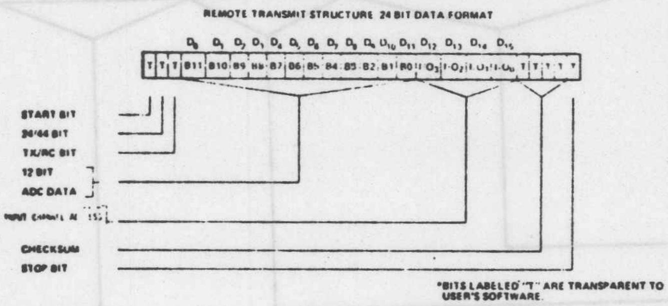
D_0-D_7 ADDRESSES ONE OF 256 REMOTES. D_0 (A7) IS MOST SIGNIFICANT BIT (MSB) AND D_7 (A0) IS LEAST SIGNIFICANT BIT (LSB).

CONTROL

D_8 = 0 DON'T PROGRAM OUTPUTS WITH D_{12}-D_{15}.
D_8 = 1 DO PROGRAM OUTPUTS WITH D_{12}-D_{15}

D_9	D_{10}	D_{11}	FUNCTION - TYPE OF RESPONSE REQUESTED
0	0	0	TRANSMISSION ERROR
0	0	1	PROGRAM I/O (IF D_8 = 1), SEND STATUS MESSAGE
0	1	0	PROGRAM I/O (IF D_8 = 1), SEND CURRENT ADC AND I/O DATA
0	1	1	SEND LAST ADC AND I/O, PROGRAM I/O (NEW MUX ADDRESS) STROBE ADC
1	0	0	PROGRAM I/O (IF D_8 = 1), STROBE ADC, SEND ADC AND I/O AFTER CONVERSION IS COMPLETE
1	0	1	TRANSMISSION ERROR
1	1	0	TRANSMISSION ERROR
1	1	1	TRANSMISSION ERROR

'Figure 4 24 BIT ANALOG REMOTE STATION COMMAND MESSAGE FORMAT.



ADC READING

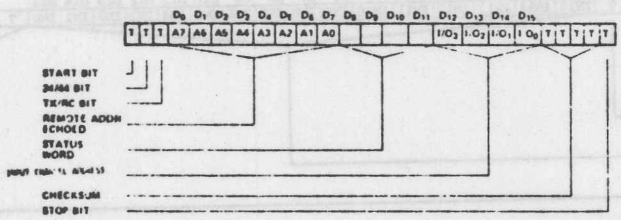
D_0-D_{11} REPRESENTS THE 12 BIT DUAL SLOPE ANALOG TO DIGITAL CONVERTER (DSADC) BINARY OUTPUTS RETURNED AS REQUESTED IN COMMAND MESSAGE SENT BY RECEIVER TRANSMITTER. D_0 (B11) CORRESPONDS TO DSADC MSB AND D_{11} (B0) CORRESPONDS TO DSADC LSB.

I/O

D_{12}-D_{15} REPRESENT STATE OF FOUR I/O LINES.

Figure 5. BIT ANALOG REMOTE STATION DATA RESPONSE MESSAGE FORMAT

REMOTE TRANSMIT STRUCTURE-24 BIT STATUS FORMAT



ADDRESS

BITS D_0-D_7 REPRESENT REMOTE'S ADDRESS: D_0 (A7) IS MSB AND D_7 (A0) IS LSB

POWER FAIL

IF D_8 = "1" THEN POWER FAILURE HAS OCCURRED AT REMOTE SINCE LAST STATUS REQUEST

D_8	$D_{1?}$	D_{11}	FUNCTION
0	0	1	LAST WORD RECEIVED BEFORE STATUS REQUEST RECOGNIZED HAD AN ILLEGAL 24/44 BIT SETTING OR LAST WORD WAS FROM ANOTHER REMOTE (TX RC BIT = 1)
0	1	0	LAST WORD WAS NOT RIGHT ADDRESS (D_0-D_7)
1	0	0	LAST WORD RECEIVED HAD CHECKSUM OR FRAMING ERROR
0	0	0	STATUS OK - LAST WORD RECEIVED WAS TO THIS STATION AND ERROR FREE

Figure 6. 24 BIT ANALOG REMOTE STATION STATUS RESPONSE MESSAGE FORMAT

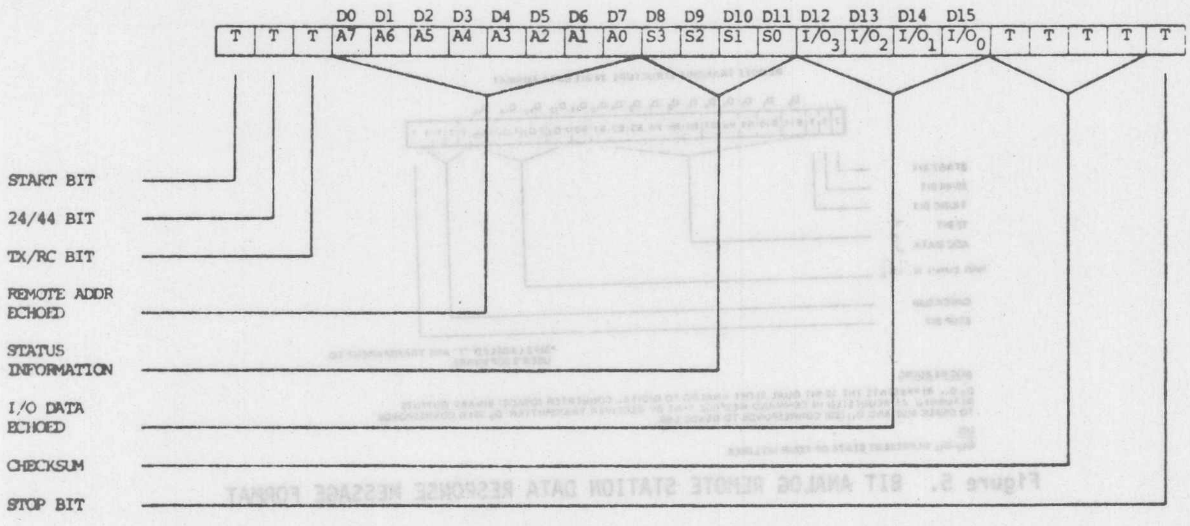


Figure 7. 24 BIT DIGITAL REMOTE STATION COMMAND MESSAGE FORMAT

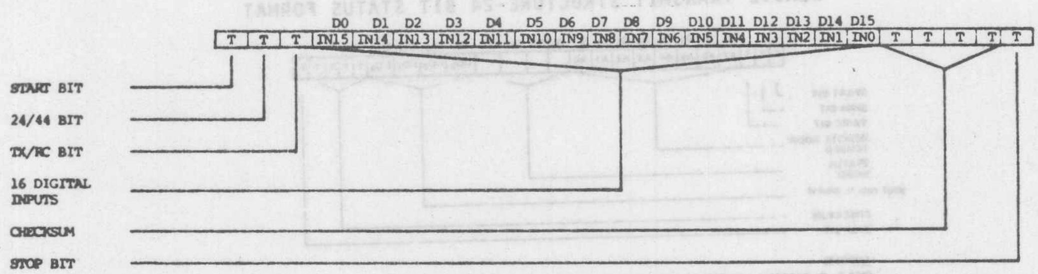


Figure 8. 24 BIT DIGITAL REMOTE STATION DATA RESPONSE MESSAGE FORMAT

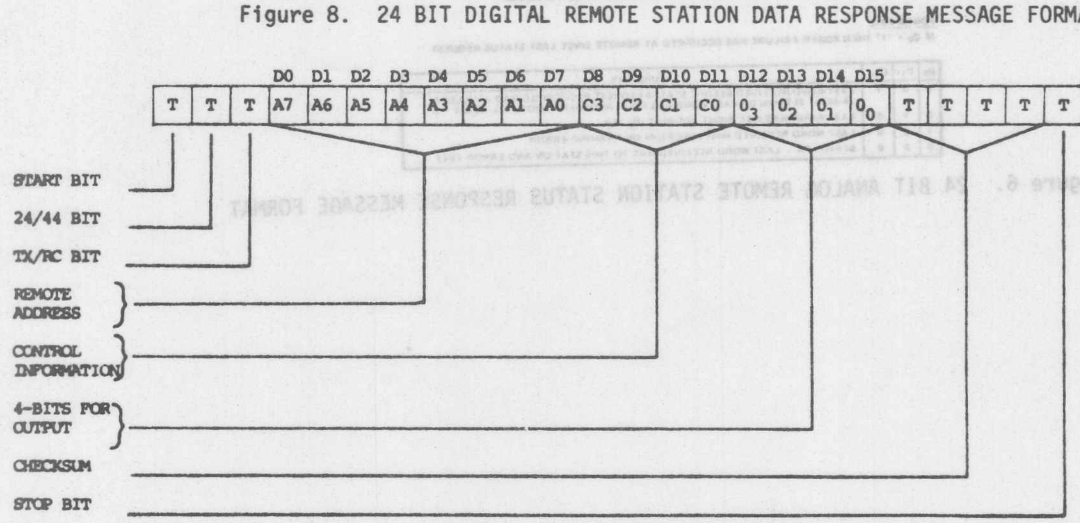


Figure 9. 24 BIT DIGITAL REMOTE STATION DATA RESPONSE MESSAGE FORMAT